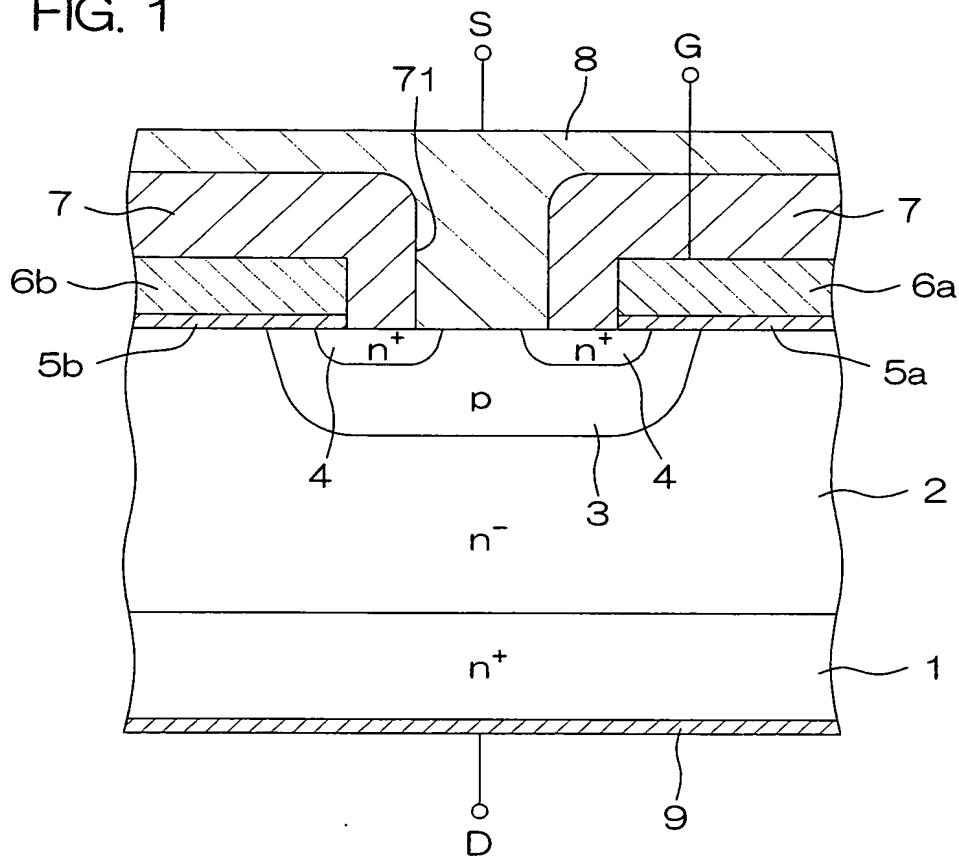


FIG. 1



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FIG. 2

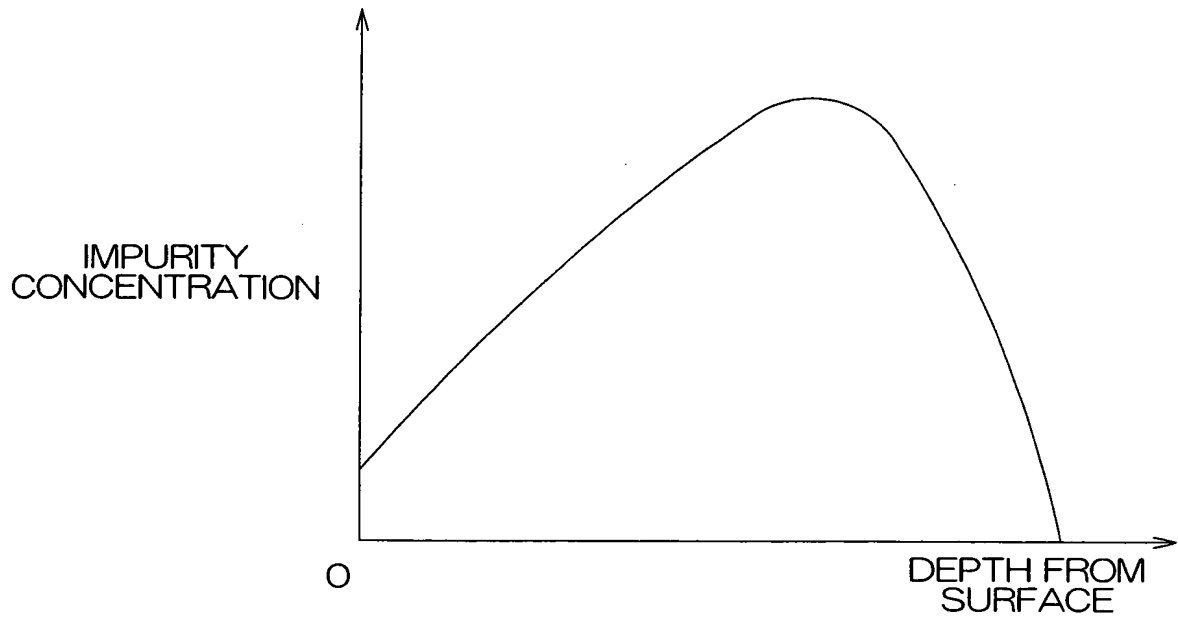
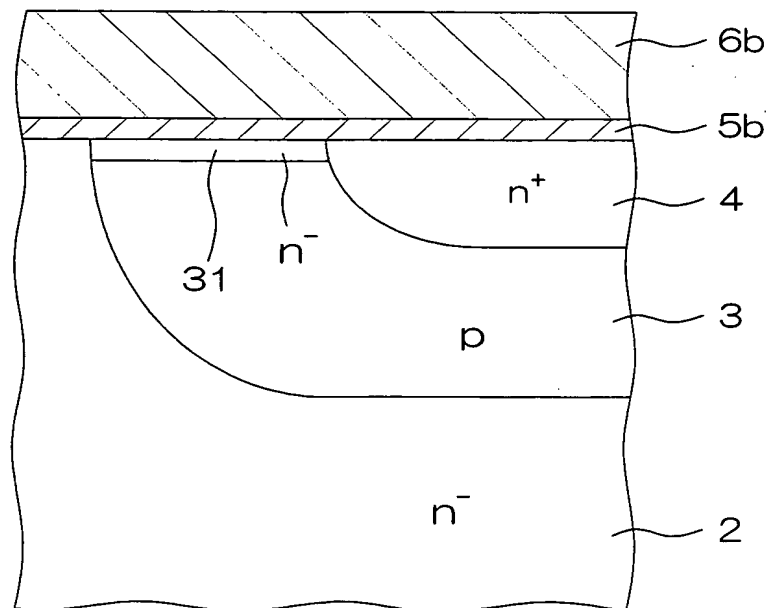


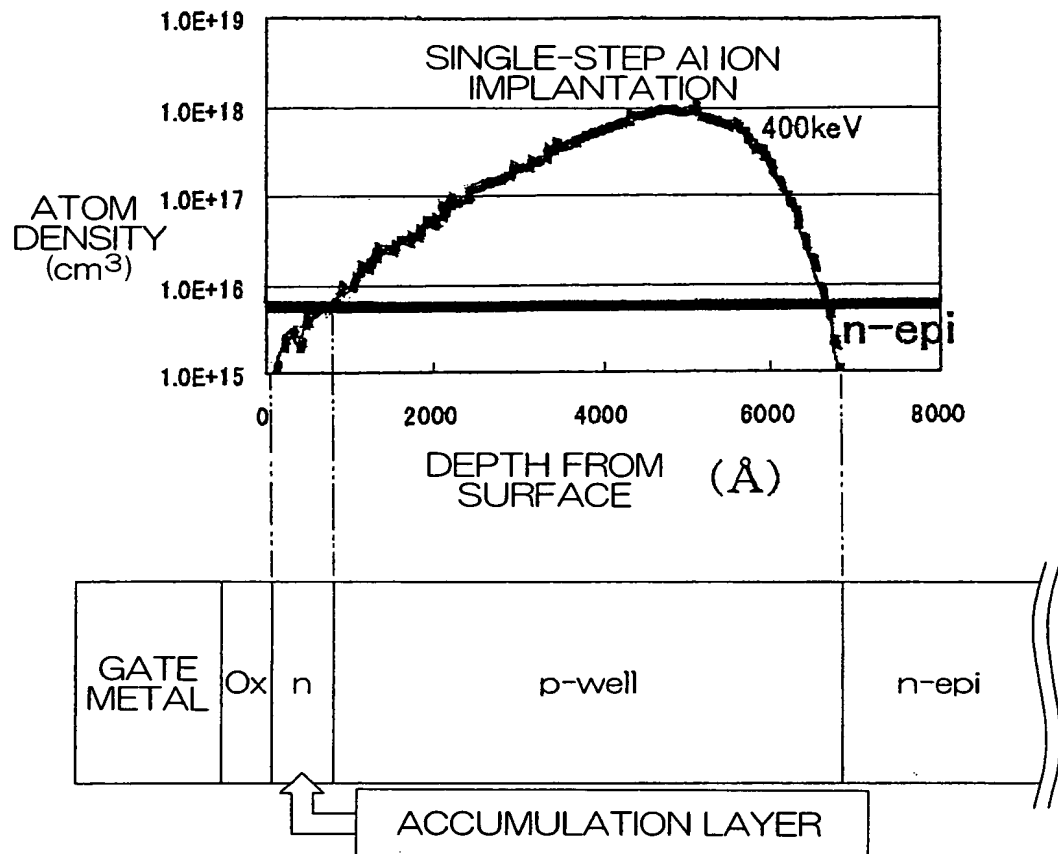
FIG. 3



A cross-sectional view of a semiconductor device. The device is built on a substrate 11. A layer 12 is on top of the substrate. A layer 13 is on top of layer 12. Layer 13 contains three regions: 14 (n+), 16 (n), and 15 (n+). A gate stack 19 is on top of region 16, with gate 20 and spacers 17 and 18. Source 17 and drain 18 are on top of regions 14 and 15 respectively. A gate 19 is on top of region 16. The device is connected to S, G, and D terminals.

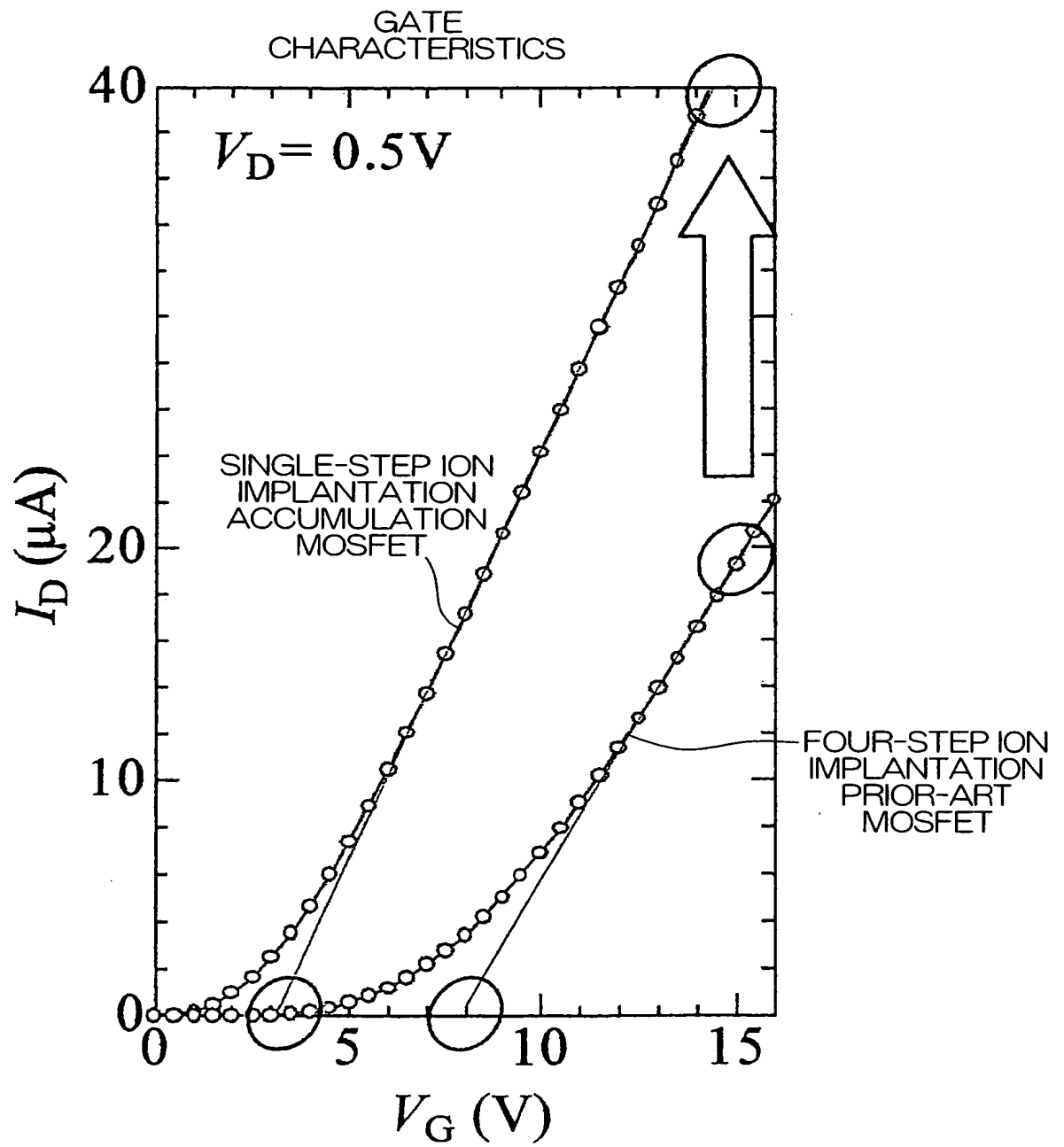
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FIG. 5



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FIG. 6



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FIG. 7

